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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/074,019	02/14/2002	Ken Cameron	0120-023	5665

42015 7590 06/11/2010

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ART UNIT	PAPER NUMBER
2443	

NOTIFICATION DATE	DELIVERY MODE
06/11/2010	ELECTRONIC

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/074,019
Filing Date: February 14, 2002
Appellant(s): CAMERON, KEN

Krishna V. Kalidinidi
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed March 22, 2010 appealing from the Office action mailed April 21, 2010.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal, is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments

The statement of the status of the Amendment contained in the brief is correct.

(5) Summary of claimed subject matter

The summary of the claimed subject matter is contained in the brief is correct.

(6) Grounds of Rejection to be reviewed on appeal

The following ground(s) of rejection are applicable to the appealed claims:

A. Claims 1-9 and 11-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Chang et al (U.S. 6,338,078 B1).

This rejection is set forth in a prior office action, mailed on April 21, 2009.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

U.S. 6,338,078 B1	Chang et al.	01-2002

(9) Grounds of Rejection

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 9 & 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (U.S. 6,338,078).

3. As per claims 1, 5 & 8 Chang disclosed a processing system comprising a plurality of processing engines for processing datagrams in a predetermined order, each processing engine comprising at least one input port, at least one output port and a plurality of processing elements, each processing element comprising an input port connected to the at least one input port of the processing engine, an output port connected to the at least one output port of the processing engine (col.5, lines 8-25) and arithmetic and logic means, and a ticket dispenser adapted to associate a ticket with each incoming datagram (col.5, lines 66-67 & col.6,lines 1-32) wherein the processing elements, upon becoming available, take a next ticket from the ticket dispenser (col.6,

lines 33-50, 66-67 & col.7, lines 1-5), an the order of processing datagrams being controlled at the at least one input port of the processing engine and at the least one output port of the processing engine in dependence on ticket associated with the datagram or a group of the datagrams and the reading and writing of the read and processed datagram takes place upon the process being given permission to continue (col.5, lines 66-67, col.6, lines 1-50). Although Chang did not explicitly disclose a ticket dispenser adopted to associate a ticket with each incoming datagram. However Chang disclosed a "hashing mechanism" (equivalent to a "ticket dispenser") that queues packets (datagrams) in a such a way that packets arrive at the device driver in a certain sequence (I.E value or number or weight or priority) and are then aligned according to that sequence to be processed by multiple processors (Figure.3, col.5, lines 8-26, lines 66-67, col.6, lines 1-32).

It would have been obvious to one in the ordinary skill in the art at the time the invention was made to have incorporated the use of "hashing mechanism" as disclosed by Chang instead of a "ticket dispenser" to align packets in a certain sequence to be processed by multiple processors in order to make the processing of the packets more efficient resulting in a more robust packet processing system.

4. As per claim 2 Chang disclosed a method according to claim 1, wherein the order of the datagrams or group of datagrams at the at least one input port corresponds to the order of the datagrams at the at least one output port (col.5, lines 66-67, col.6, lines 1-50).

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5. As per claim 3 Chang disclosed a method according to claim 1, wherein the tickets comprise numerical values (col.5, lines 66-67, col.6, lines 1-50).

6. As per claim 4 Chang disclosed a method according to claim 1, wherein the ticket comprises a semaphore with data associated therewith (col.5, lines 66-67, col.6, lines 1-50).

7. As per claim 6 Chang disclosed a processing engine according to claim 5, wherein the processing element comprises an element of a multi threaded array processing engine (col.5, lines 1-26)

8. As per claim 7 Chang disclosed a processing engine according to claim 5, wherein the processing element can leave or enter the predetermined order (col.5, lines 66-67 & col.6, lines 1-32).

9. As per claims 9 Chang disclosed a processing system according to claim 8, wherein datagrams are processed in a round robin manner (col.6, lines 15-33 & col.7, lines 49-55).

10. As per claim 11 Chang disclosed a processing system according to claim 10, wherein the tickets are issued on a first come first served basis ((col.5, lines 1-26, lines 66-67 & col.6, lines 1-50).

11. As per claim 12 Chang disclosed a processing system according to claim 8 further comprising a counter for maintaining the value of the current ticket (col.5, lines 66-67 & col.6, lines 1-50).

12. As per claim 13 Chang disclosed a processing system according to claim 12, wherein the counter comprises storage means for storing a numerical value (col.5, lines 66-67 & col.6, lines 1-50).

13. As per claim 14 Chang disclosed a processing system according to claim 13, wherein once a processing element is allocated a datagram or group of datagrams for processing, the counter is incremented (col.5, lines 66-67 & col.6, lines 1-50).

14. As per claim 15 Chang disclosed the method of claim 1, wherein a number of tickets is greater than a total number of processors (col.5, lines 14-17).

15. As per claim 16 Chang disclosed the method of claim 1, wherein the ticket represents an arrival time of the packet (col.6, lines 4-50).

16. As per claim 17 Chang disclosed the method of claim 1, wherein the processor drops selected datagrams from being written to the output buffer (col.6, lines 4-50).

17. As per claim 18 Chang disclosed the method of claim 1, wherein the processor enters or leaves a processing sequence (col.5, lines 29-39).

(10) Response to Arguments

With respect to claims 1-9 and 11-18 appellant argued on the following limitations against the applied prior art Chang et al (U.S. 6,338,078 B1)

A. The rejection of claims 1-9 and 11-18 under 35 U.S.C 103 (a) as allegedly being unpatentable over Chang should be reversed.

(i) Independent claim 1

Issue 1: Appellant on the second last paragraph argued that Chang failed to disclose the features taken by the processor based on the value associated with the ticket dispenser by the processor and on last paragraph of page 6 copied the following limitations of claim 1 (i) "waiting on an input buffer of the input port until the processor is given permission to continue according to the value of the ticket taken"; (ii) "reading a next datagram or group of datagrams once the processor is given permission to continue"; (iii) "waiting on an output buffer of the output port until the processor is given permission to continue according to the value of the ticket taken"; and (iv) "writing the processed datagram once the processor is given permission to continue"

and alleged that Chang fails to teach them. Additionally, appellant argued various limitations of claim 1 from pages 7 though 9.

As to appellant's argument in order to clearly present to the board how Chang anticipates claim 1 examiner will address claim 1 in its entirety with supporting excerpts from the prior art Chang with an explanation.

"*A method for controlling the order of datagrams, the datagrams being processed by at least one processing engine, said at least one processing engine having at least one input port and at least one output port*"

Chang discloses multiple processors (MP) having input and output ports that processes the packets (A.K.A datagrams) in a sequence (by keeping them in order I.E controlling their order) (Figure. 3 and col.2, lines 55-67 and col.3, lines 1-6)

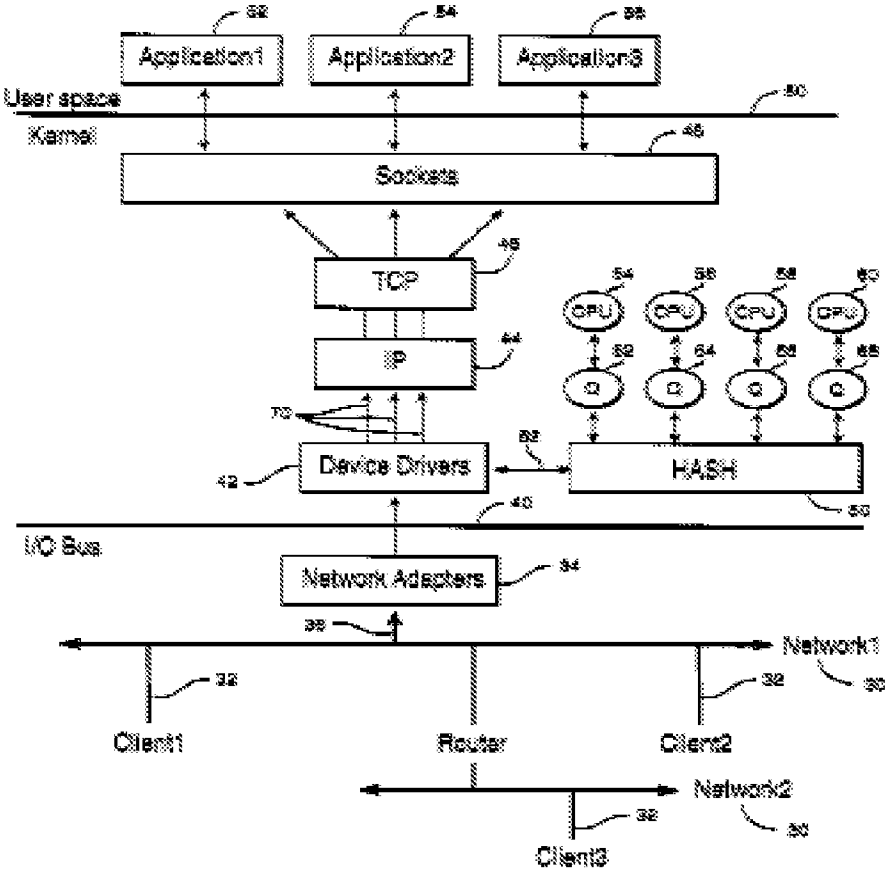

FIG. 3

Network input processing is distributed to multiple CPUs on multiprocessor systems to improve network throughput and take advantage of MP scalability. Packets received on the network are distributed to N high priority threads, wherein N is the number of CPUs on the system. N queues are provided to which the incoming packets are distributed. When one of the queues is started, one of the threads is scheduled to process packets on this queue. When all of the packets on the queue are processed, the thread becomes dormant. Packets are distributed to one of the N queues by using a hashing function based on the source MAC address, source IP address, or the packet's source and destination TCP port number, or all or a combination of the foregoing. The hashing mechanism ensures that the sequence of packets within a given communication session will be preserved. Distribution is effected by the device drivers of the system Parallelism is thereby increased on network I/O processing, eliminating CPU bottleneck for high speed network I/Os, thereby improving network performance.

" the method comprises the steps of:
(a) each processor in the at least one processing engine, once it becomes available, taking a ticket from a ticket dispenser, the ticket having a value associated therewith;
(b) waiting on an input buffer of the input port until the processor is given permission to continue according to the value of the ticket taken in step"

Change in figure 3 disclosed "Hash function" (Element 50) in communication with the Device Drivers (Element 42) that performs the equivalent functionality of the "ticket dispenser" {analogy and motivation indicated in the Final office action un 35 U.S. C 103(a)} (Figure.1 and col.6, lines 33-50)

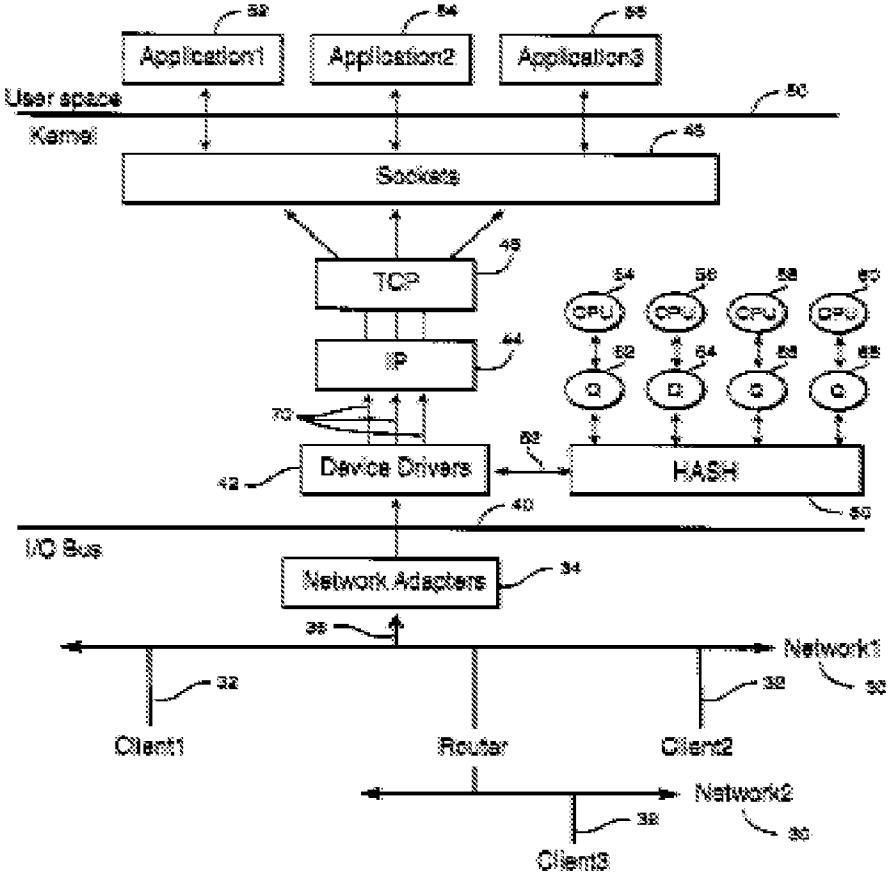

FIG. 3

Chang disclosed the “Hash function” (I.E “ticket dispenser”) where datagrams/packets are assigned a priority (I.E ticket) {described above in col.2, lines 55-67} and are then dispensed to N priority threads/queues (elements 62, 64, 66 and 68) where they wait to get processed by the processors (Elements 54, 56, 58 and 60) according to their priority (I.E ticket). (col.6, lines 15-50)

Techniques exist for ensuring packets being received from a client are sequenced properly regardless of whether in the conventional TCP/IP or other network protocol form. The subject invention applies this sequencing in the context of improved parallelization of multiple CPUs in a network system. Thus, referring to FIG. **3** in greater detail, additional functionality is provided, extended from the driver to a queuing mechanism which runs on multiple threads. These queues may be seen at reference numeral **62, 64, 66, 68** with, in a multithreaded fashion, a plurality of different CPU engines schematically depicted by CPUs **54, 56, 58, 60** of an MP system running on them. The invention provides a sequencing to the packets received by the device drivers **42** so that as they proceed through the protocol stacks of FIG. **4** they arrive in sequence. In the FIG. **3**, the number of queues **62–68** provided, equal the number of CPUs **54–60** so that these multiple CPUs can be simultaneously working to process packets.

As in conventional systems, each packet has its own unique address. In one implementation of the invention, advantage is taken of the fact that media access control (MAC) addresses may be utilized for this hashing and sequencing as in the familiar Ethernet. Each network interface card (NIC) conventionally may have, for example, a 24 bit MAC, with each packet associated therewith having a like MAC address. It is a feature of the invention to hash, in accordance with the hash function **50** shown in FIG. **3**, each of these MACS into the aforementioned plurality of queues **62–68**, whereby a hash provided by the hash function **50** to packets in the device drivers **42** by means of the interconnection **52** will occur for given devices to the network so that packets associated with a given device will be handled in the same particular queue. Therefore no matter which CPU **54–60** handles a particular queue, the packets associated with a particular device will flow to one of the applications **52–56** in sequence.

"(c) reading a next datagram or group of datagrams once the processor is given permission to continue;
(d) signaling the input buffer for next ticket value;
(e) processing the read datagram by the processor;"

The limitations comprising **steps (c) through (e) above are merely the repetition of steps (a) and (b)** and it is basically saying that as more datagrams arrive they too go through the same process as explained above.

"(f) waiting on an output buffer of the output port until the processor is given permission to continue according to the value of the ticket taken in step (a);"

The above limitation (f) is **simply describing an inherent fact** that is universally present in all processors. Of course a processor in general has limitations as to how many datagrams it can process **at a given instant** and send them out through its output buffer. In other words **a processor cannot process an unlimited number of datagrams at a given instant**. Therefore it holds back the processing of the remaining datagrams until becomes free to process the next set of datagrams that it is able to process. Processing of datagrams is disclosed by Chang in the excerpts and in figure 1 described above.

"(g) writing the processed datagram once the processor is given permission to continue;"

This step is again describing the **inherent functionality** that once processor is allowed to process the datagram, the datagram is processed and it is written in the output buffer of the processor to proceed to its next level in the OSI model.

(h) signaling the output buffer for next ticket value; and

Chang discloses that the datagrams are processed in order therefore once one datagram is processed the next datagram in accordance with the hash value described by Chang is slated to be processed by the processor.

(i) repeating steps (a)-(h) for each ticket value.

The above steps simply repeats the steps described above.

Therefore Chang clearly discloses claim 1.

Issue 2: On the second paragraph of page 9 appellant argued that independent claims 5 and 8 are allowable foe the same reasons given for claim 1.

As to appellant's argument, examiner has addressed all the limitations of claim 1 that are also common in claims independent 5 and 8 by Chang. Since claim 1 is not allowable in light of Chang's disclosure therefore claims 5 and 8 are also not allowable.

(ii) Dependent claims 2-4 and 15-18

Issue 1: Appellant on page 9 argued that dependent claims 2-4 and 15-18 are allowable for the same reason given for claim 1 to be allowable since they depend on claim1.

As to appellant's argument since claim 1 is not allowable as explained by the examiner above therefore its dependent claims 2-4 and 15-18 are also not allowable for the same reason given by the examiner.

(iii) Dependent claims 6 and 7

Issue 1: Appellant on page 9 argued that dependent claims 6 and 7 are allowable for the same reason given for claim 5 to be allowable since they depend on claim 5.

As to appellant's argument since claim 5 is not allowable as explained by the examiner above therefore its dependent claims 2-4 and 15-18 are also not allowable for the same reason given by the examiner.

(iv) Dependent claims 9 and 11-14

Issue 1: Appellant on page 10 argued that dependent claims 9 and 11-14 are allowable for the same reason given for claim 8 to be allowable since they depend on claim 8. As to appellant's argument since claim 8 is not allowable as explained by the examiner above therefore its dependent claims 2-4 and 15-18 are also not allowable for the same reason given by the examiner.

Examiner believes that the rejection based on prior art references is proper, sustainable and clearly anticipate applicant's invention as claimed and should be affirmed.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related proceedings appendix

None.

Respectfully submitted,

/Asghar Bilgrami/

Examiner, Art Unit 2243

May 25, 2010

Conferees:

/George C Neurauter, Jr./
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